Government College of Engineering, Aurangabad
(An Autonomous Institute of Government of Maharashtra)

T. E. (EEP) Examination
End Semester Examination

EE 342: DIGITAL ELECTRONICS

17 NOV 2016

Time: Three Hours *Max Marks: 60*

"Verify the course code and check whether you have got the correct question paper"

N.B:-

1. *Attempt **all** questions*
2. *Each question carries 12 marks*
3. *Assume suitable data if necessary and state it clearly*
4. ***Use of programmable calculator is not allowed***

Q.1a) Which is the fastest saturated logic family? What feature of the family make it fastest? Explain your answer with circuit diagram. (4)

b) Multiply $(345)_8$ and $(267)_8$. (2)

c) Perform $(E631)_H - (48BD)_H$. (2)

d) Using NOR gates, implement the circuit to get output Y = (A+B) (C+D). (2)

e) Find the octal equivalent of the hexadecimal number AB.CD (2)

Q.2a) Using the tabular method, simplify the SOP expression for the Boolean function

$Y = \sum m\ (1,3,4,5,7,9,12,13)$

Draw a logic diagram using NAND gates. (6)

b) A combinational switching circuit has 4 inputs and one output. The output is 0, if any 3 or 4 of the inputs are 0. Using K-map, implement the circuit with minimum number of NAND gates. (6)

Q.3 Attempt **any two**

a) What do you understand by quantization error in analog to digital converters? Explain the principle of parallel comparator type analog to digital converter. (6)

b) Explain in detail successive approximation type analog to digital converter. (6)

c) What do you understand by programmable logic devices? Discuss with necessary diagram, the functioning of complex programmable logic devices. (6)

Q.4 Attempt **any two**

a) Discuss 4-bit parallel up-down counter with a control line for up and down counting. Explain the operation with waveforms. (6)

b) Using D-flip-flop design synchronous counter that progresses through following sequence-

0000, 1000, 0110, 1001, 0001, 0010, 0000…

Draw its timing diagram. (6)

c) What is meant by multiplexer? (6)

Realize the logic circuit using 8:1 multiplexer for the truth table shown below-

Inputs				Output
A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Q.5 Write short notes on (**any three**) (12)

a) Bidirectional Shift Register

b) Field Programmable Gate Array

c) PROM

d) R-2R Ladder type DAC

e) Ring Counter